CLAIMS

What is claimed is:

1. A memory device for use with a memory controller, the memory device comprising:

a memory cell array adapted to store internal depth data of an object; and

a data modifying circuit distinct from the memory controller, the data modifying circuit being adapted to

receive corresponding new external depth data of the object from the memory controller,

compare the new external depth data with the internal depth data, and

write the external depth data in the memory cell array over the internal depth data depending on the result of the comparison.

2. The memory device of claim 1, wherein

the data modifying circuit is further adapted to output to the memory controller a status signal.

3. The memory device of claim 1, further comprising:

a first control pin for receiving a first control signal from the memory controller; and

a control circuit for transmitting the external depth data to the memory cell array thereby bypassing the data modifying circuit depending on a state of the first control signal.

4. The memory device of claim 3, wherein

the data modifying circuit is further adapted to output to the memory controller a status signal.

5. The memory device of claim 4, wherein

the status signal is output through the first control pin.

6. The memory device of claim 1, wherein the data modifying circuit includes

a register for storing the received new external depth data; and

a compare circuit for comparing the stored new external depth data with the internal depth data and for writing the external depth data in the memory cell array depending on the result of the comparison.

7. The memory device of claim 6, wherein

the compare circuit is further adapted to write the external depth data in the memory cell array if the external depth data is smaller than the internal depth data.

8. The memory device of claim 6, wherein

the compare circuit is further adapted to output a status signal to the memory controller.

9. The memory device of claim 6, further comprising:

a second control pin for receiving a second control signal from the memory controller,

wherein the compare circuit compares the internal depth data with the stored external depth data in units of X bits when the second control signal is in a non-active state, and in units of NX bits when the second control signal is in an active state.

10. The memory device of claim 9, wherein

if the second control pin is in an inactive state, the compare circuit outputs to the memory controller:

a first status signal indicating that the lower X bits of the internal depth data have been modified, and

a second status signal indicating that the upper X bits of the internal depth data have been modified.

11. The memory device of claim 9, wherein

if the second control pin is in a non-active state, the compare circuit outputs to the memory controller a status signal indicating that NX bits of the internal depth data have been modified.

12. A method of processing depth data of an object in a memory device controlled by a memory controller, the method comprising the steps of:

(a) receiving external depth data of the object from the memory controller;

(b) storing the received external depth data;

(c) receiving a first control signal from the memory controller through a first control pin distinct from the memory controller;

(d) determining a state of the first control signal; and

(e) if the state of the first control signal is determined to be inactive, writing the external depth data to a memory cell array within the memory device,

(f) elseif the state of the first control signal is determined to be active, comparing the stored external depth data with corresponding internal depth data stored in the memory cell array, and writing the external depth data over the corresponding internal depth data in the memory cell array depending on the result of the comparison.

13. The method of claim 12, wherein

step (f) further includes outputting to the memory controller a status signal indicating that the internal depth data has been modified.

14. The method of claim 12, wherein

writing in step (f) takes place if the comparison yields that the external depth data is smaller than the internal depth data.

15. The method of claim 12, wherein

writing in step (f) takes place if the comparison yields that the external depth data is larger than the internal depth data.

16. The method of claim 12, further comprising:

(g) receiving a second control signal from the memory controller through a second control pin distinct from the memory controller;

(h) determining a state of the second control signal; and

(i) if the state of the second control signal is determined to be inactive, comparing the internal depth data with the stored external depth data in units of X bits,

(j) elseif the state of the second control signal is determined to be active, comparing the internal depth data with the stored external depth data in units of NX bits.

17. The method of claim 16, wherein step (i) further includes

outputting to the memory controller a first status signal indicating that the lower X bits of the internal depth data have been modified, and

outputting to the memory controller a second status signal indicating that the upper X bits of the internal depth data have been modified.

18. The method of claim 17, wherein
the first status signal is output through the first control pin, and
the second status signal is output through the second control pin.

19. The method of claim 16, wherein step (j) further includes
outputting to the memory controller a status signal indicating that the NX bits of the internal depth data has been modified.

20. The method of claim 19, wherein
the status signal is output through one of the first and second control pins.